IN THE CLAIMS

1 (Previously Presented). A method comprising:

covering a polysilicon gate structure with a hard mask to prevent the formation of a silicide on the gate structure, said mask and said gate structure having opposed, common vertical surfaces; and

forming a sidewall spacer that extends along a vertical surface and covers said gate structure and covers at least part of said mask; and

removing said hard mask using an etch that is selective of the hard mask over the spacer.

2 (Previously Presented). The method of claim 1 including protecting the polysilicon gate structure with a hard mask to prevent the formation of a silicide.

3 (Original). The method of claim 2 including protecting the polysilicon gate structure with a nitride hard mask to prevent the formation of a silicide.

4 (Previously Presented). The method of claim 1 including selectively protecting at least one polysilicon gate structure with the mask to prevent the formation of a silicide and removing the mask over another gate structure to form a silicide on the another gate structure.

5 (Original). The method of claim 1 including removing said mask after forming a silicide.

6 (Original). The method of claim 5 including removing said mask by etching.

7 (Original). The method of claim 5 including removing said mask by polishing.

8 (Original). The method of claim 5, including polishing said mask then etching said mask.

9 (Original). The method of claim 1 including replacing the polysilicon gate structure with a metal gate replacement.

10 (Original). The method of claim 1 including forming the polysilicon gate structure including a patterned polysilicon portion and an underlying dielectric layer.

11 (Original). The method of claim 10 including protecting the underlying dielectric layer from overetching.

12 (Original). The method of claim 1 including forming spacers on either side of said polysilicon gate structure to prevent lateral silicide formation.

13 (Original). The method of claim 5 including using a two-step polish to remove said mask including a first step using a harder pad and a second step using a softer pad.

Claims 14-19 (Canceled).

20 (Withdrawn). A semiconductor wafer comprising:

a semiconductor substrate;

a first polysilicon gate structure formed over said semiconductor substrate;

a second polysilicon gate structure formed over said semiconductor substrate; and

a mask over said first polysilicon gate structure and said second polysilicon gate structure being maskless.

21 (Withdrawn). The wafer of claim 20 wherein said mask is a hard mask.

22 (Withdrawn). The wafer of claim 21 wherein said mask is a nitride hard mask.

23 (Withdrawn). The wafer of claim 20 including a dielectric layer between said gate structures and said semiconductor substrate.

24 (Withdrawn). The structure of claim 20 wherein said second gate structure has silicide formed thereon and said first gate structure is substantially free of silicide.

25 (Previously Presented). The method of claim 14 wherein said hard mask is nitride.

26 (Previously Presented). The method of claim 25 wherein said first polysilicon structure includes sidewall spacers.

27 (Previously Presented). The method of claim 26 wherein an etch is used that is selective of said nitride.

28 (Previously Presented). The method of claim 27 including using H_3PO_4 to etch said mask.